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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 6,952,018 B2)
MEARS ET AL.)

Issued: October 4, 2005)

For: SEMICONDUCTOR DEVICE INCLUDING)
BAND-ENGINEERED SUPERLATTICE)

Certificate
FEB 02 2006
of Correction

REQUEST FOR CERTIFICATE OF CORRECTION OF
APPLICANT'S MISTAKE UNDER RULE 1.323

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of Rule 1.323 of the Rules of Practice, the Patent Office is respectfully requested to correct matters in the above-identified patent in accordance with the Certificate of Correction Form PTO-1050 attached hereto.

The Patent Office is requested to issue a Certificate of Correction on the above-referenced Patent Document, and to place such a Certificate of Correction in the file, so that such will appear on any copies of the patent which are ordered in the future.

The corrections being made are of consequence to provide the proper recitation on the face of the patent, in the drawings, specification, and claims. Several of the mistakes occurred in good faith and are not the fault of the Patent and Trademark Office. However, a couple printing errors of the Patent Office are also being corrected. No new matter is added by these corrections.

01/30/2006 SSESHE1 00000038 6952018

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FEB 03 2006

In re Patent of
MEARS ET AL.
Patent No. 6,952,018 B2
Issued: October 4, 2005

The Commissioner is hereby authorized to charge the requisite fee as set forth in 37 CFR § 1.20(a) in the amount of \$100.00 to the credit card noted in the attached credit card payment form. The Commissioner is authorized to charge or credit any discrepancies in fee amounts to Deposit Account 01-0484.

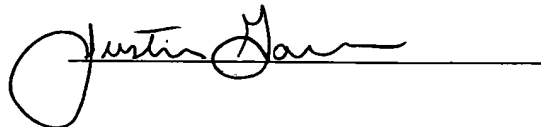
Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 23rd day of January, 2006.



FEB 03 2006

CERTIFICATE OF CORRECTION

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below

FEB 03 2006

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	:	6,952,018 B2
DATED	:	October 4, 2005
INVENTOR(S)	:	Mears et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below

Column 3, Line 4 Delete: "as may"
 Insert: --as may be--

Column 4, Line 30 Delete:

$$M_{h,i,j}^{-1}(E_F, T) = \frac{- \sum_{E > E_F} \int_{B.Z.} (\nabla_k E(k, n))_i (\nabla_k E(k, n))_j \frac{\partial f(E(k, n), E_F, T)}{\partial E} d^3 k}{\sum_{E > E_F} \int_{B.Z.} f(E(k, n), E_F, T) d^3 k}$$

 Insert:

$$M_{h,i,j}^{-1}(E_F, T) = \frac{- \sum_{E < E_F} \int_{B.Z.} (\nabla_k E(k, n))_i (\nabla_k E(k, n))_j \frac{\partial f(E(k, n), E_F, T)}{\partial E} d^3 k}{\sum_{E < E_F} \int_{B.Z.} (1 - f(E(k, n), E_F, T)) d^3 k}$$

Column 5, Line 11 Delete: "gate 35"
 Insert: --gate 38--

Column 5, Line 60 Delete: "gate 35"
 Insert: --gate 38--

Column 7, Line 63 Delete: "from the both"
 Insert: --from both--

Column 9, Lines 44-46 Delete: "In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer."

MAILING ADDRESS OF SENDER:

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Column 9, Line 59	Delete: "also formed" Insert: --also be formed--
Column 10, Line 58	Delete: "claim 3 the" Insert: --claim 3 wherein the--
Column 12, Line 15	Delete: "claim 19 the" Insert: --claim 19 wherein the--
Column 12, Line 19	Delete: "wherein wherein" Insert: --wherein--

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